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STDP implementation using memristive nanodevice in CMOS-Nano neuromorphic networks

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Abstract: Implementation of a correlation-based learning rule, Spike-Timing-Dependent-Plasticity (STDP), for asynchronous neuromorphic networks is demonstrated using 'memristive' nanodevice. STDP is performed using locally available information at the specific moment of time, for which mapping to crossbar-based CMOS-Nano architectures, such as CMOS-MOLecular (CMOL), is done rather easily. The learning method is dynamic and online in which the synaptic weights are modified based on neural activity. The performance of the proposed method is analyzed for specifically shaped spikes and simulation results are provided for a synapse with STDP properties.

Keywords: CMOL, memristive, neuromorphic networks, STDP learning

Classification: Electron devices, circuits, and systems

References

[1] O. Turel, J. H. Lee, X. Ma, and K. K. Likharev, "Neuromorphic architectures for nanoelectronic circuits," *Int. J. Circuit Theory Appl.*, vol. 32, pp. 277–302, 2004.

[2] T. Oya, A. Schmid, T. Asai, Y. Leblebici, and Y. Amemiya, "On the fault tolerance of a clustered single-electron neural network for differential enhancement," *IEICE Electron. Express.*, vol. 2, no. 3, pp. 76–80, 2005.

[3] G. Indiveri, E. Chicca, and R. Douglas, "A VLSI array of low-power spiking neurons and bistable synapses with spike-timing dependent plasticity," *IEEE Trans. Neural Netw.*, vol. 17, pp. 211–221, 2006.

[4] G. Bi and M. Poo, "Synaptic modification by correlated activity: Hebb's postulate revisited," *Annual Review of Neuroscience*, vol. 24, pp. 139–166, 2001.

[5] M. Masoumi, F. Raissi, M. Ahmadian, and P. Keshavarzi, "Design and evaluation of basic standard encryption algorithm modules using nano-sized complementary metal oxide semiconductor molecular circuits," *Nanotechnology*, vol. 17, pp. 89–99, 2006.

[6] G. S. Snider, "Spike-Timing-Dependent learning in Memristive Nanodevices," *IEEE/ACM International Symposium on Nanoscale Architectures*, Anaheim, CA, pp. 85–92, June 2008.

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[7] A. Gorchetchnikov, M. Versace, and M. E. Hasselmo, "A model of STDP based on spatially and temporally local information: Derivation and combination with gated decay," *Neural Networks*, vol. 18, pp. 458–466, 2005.
[8] W. Gerstner, R. Kempter, J. L. van Hemmen, and H. Wagner, "Hebbian learning of pulse timing in the Barn Owl auditory system," *Pulsed neural networks*, ed W. Maass and C. M. Bishop, pp. 353–377, MIT Press, Cambridge, MA, 1999.

1 Introduction

Hybrid CMOS-Nano architectures, such as CMOL [1], provide massive parallelism and high density for developing fault and defect tolerant neuromorphic networks (NNs) [2]. The implementation of NNs in such architectures, however, would involve modifications compared to regular CMOS implementations. For example, regular implementation of correlation-based learning rules by storage of spike timing in a certain window using a capacitor per synapse [3] is impossible in such hybrid architectures, due to lack of one-to-one connectivity between neurons. The challenge is to implement correlation-based learning laws, such as STDP [4], based on the state of a two-terminal nanodevice for long-term potentiation (LTP) (for pre-before-postsynaptic spiking) and long-term depression (LTD) (for post-before-presynaptic spiking) as well as state storage.

Conventional CMOL circuits [1, 5] comprise bistable single-electron devices (SEDs) whose behavior are like single bit Resistance-change RAMs (ReRAMs). But, the resistance of recently fabricated nanodevice, 'memristive' [6], is nonlinear and varying between "On" (low resistance) state and "Off" (high resistance) state by applying appropriate voltages. Thus, the memristive nanodevice can function as analog devices, which lets it perform as a continuous weight synapse.

Using memristive nanodevice, Snider has proposed self-organized computation and STDP implementation in a synchronous paradigm, see [6] and reference [19] therein. NNs which use spiking neurons, however, operate asynchronously to express analog information by the timing of neural spike firing, and it is expected that the asynchronous implementations operate faster than the synchronous ones. In this paper, we show a possible asynchronous implementation of STDP learning in CMOL-based NNs using memristive nanodevice. We modify a local STDP learning rule, given in [7], and verify CMOL mapping considerations and examine the learning method at cellular level.

2 CMOL-based NNs using memristive nanodevice

NNs are implemented in CMOL using CMOS circuits as neurons (somas); nanowires as axons and dendrites; and nanodevices as synapses. Fig. 1 shows the general architecture of CMOL NNs using memristive nanodevices. The nanowire crossbar is connected to the bottom CMOS neuron circuits and performs signal routing. Programmable nanodevices in CMOL circuits are

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formed at each crosspoint of the crossbar. We use the voltage-controlled memristive nanodevice, by model definition of [6], at crosspoints as a synapse whose weight variable is memristive conductance (MC). The function of the device is 'sinh-like' in the voltage, v, and it can be approximated for each value of MC by,

$$\frac{\mathrm{d\,MC}}{\mathrm{dt}} = \mathrm{A}\ \sinh(\mathrm{B\,v}) \tag{1}$$

The parameters A and B depend upon the nanodevice material, thickness, size and fabrication method. The nonlinearity is of prime importance; as well as the fact that the small voltages across the nanodevice bellow its threshold, $|V_{th}|$, do not induce much change in MC, while larger voltages induce much greater changes. The device has polarity and positive voltages increase MC, while negative voltages decrease it.

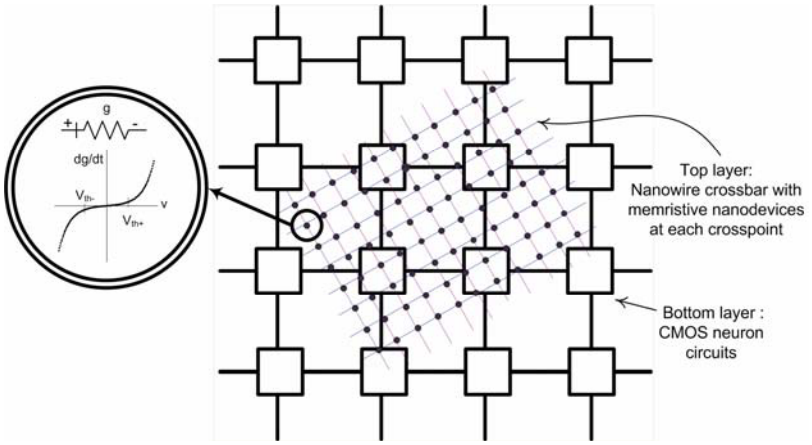

Fig. 1. Structural view of CMOL neuromorphic networks using memristive nanodevices with nonlinear conductance (g).

3 Proposed methodology

We use CMOS based spiking neuron which works basically the same as conventional Integrate-and-Fire (I&F) neurons [3], but introducing special shaped spike and specific back-propagation to adapt it to the CMOL platform, as sketched in Fig. 2 (a). The total current received by a neuron input depends on the MC of connected synapses and the voltage drop across the synapses, as Ohm's law. The sum of all input currents increases the dendritic voltage of the postsynaptic neuron until its integrator voltage (V_{soma}) reaches a threshold ($V_{threshold}$). Then the neuron fires and sends a special shaped spike forward to its axon and backward to its dendrite, simultaneously. Backward spike turns learning ON/OFF, and for non-plastic synapses, such as fixed inhibitory synapses, one does not need to establish spike back-propagation.

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3.1 Spike shape and learning analysis

Neurons in our topology fire special shaped spikes to carry the spike-timing information and to form a learning window in a process similar to that described in [8]. The spike comprises of two parts: a negative pulse followed by a positive triangular pulse, Fig. 2 (b). The spike has a shorter negative part than positive part, $d_s \ll d_l$. The longer part of the spike determines the temporal extents of the learning window. When this positive part applied to an "On" state memristive synapse creates a current pulse which increases the dendritic voltage. The negative part is used to obtain the voltage threshold needed to program the memristive nanodevice and since this part is narrow it has less effect on dendritic voltage. The spike is approximated as a piecewise linear function,

$$X = \begin{cases} V_- & V_{soma} > V_{threshold} \\ -\dfrac{V_+}{d_l}(t-s) + V_+ & s < t \leq s + d_l \\ 0 & other\ wise \end{cases} \quad (2)$$

s is the time of arrival of the spike, and V_- and V_+ are the peak amplitudes of negative and positive parts, respectively. The peak amplitudes are somewhat below memristive threshold, i.e. $|V_-|, |V_+| < |V_{th\pm}|$, to avoid too much MC change by a single spike. If any pre- and postsynaptic neurons are well synchronized, the voltage produced across the synapse located between them will provide STDP properties.

Assume that X_{pre} and X_{post} are pre- and postsynaptic spikes, respectively, and X_{pre} occurs at time $t_{pre} = 0$ and X_{post} occurs at time $t_{post} = s$, Fig. 2 (c), then $\Delta t = t_{post}\text{-}t_{pre} = t_{post} = s$. Following cases may occur depending on the time of arrival of the post- and presynaptic spikes:

- If $0 < s < d_l$ meaning that pre-before-postsynaptic spiking has happened and LTP would occur. In this case, during the d_s of X_{post} the voltage across the memristive nanodevice is greater than its positive threshold ($X_{pre}\text{-}X_{post} > V_{th+}$), Fig. 2 (d) windows (1, 2). The more synchronized the post- and presynaptic spikes, the greater the voltage and the greater the LTP (with *sinh* rate).

- If $-d_l < s < 0$ meaning that post-before-presynaptic spiking has happened and LTD would occur. In this case, during the d_s of X_{pre} the voltage across the memristive nanodevice decreases below its negative threshold ($X_{pre}\text{-}X_{post} < V_{th-}$), Fig. 2 (d) window (3).

- If two spikes are not well synchronized, i.e. $s < -d_l$ or $s > d_l$ there will be no overlap between pre- and postsynaptic spikes and MC will not change, because the voltage across the memristive nanodevice does not reach its threshold.

The spike shape has a vital role in our learning method, while CMOS circuit constraints or RC elements through routings may impact on the learning

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efficiency. We can successfully extend this method for a different spike shape with a gradual transition and an exponential decaying part, as:

$$X = \begin{cases} V_- & V_{soma} > V_{threshold} \\ \dfrac{V_+ + |V_-|}{\varepsilon}(t-s) + V_- & s < t \le s+\varepsilon \\ V_+ \exp(-(t-s-\varepsilon)/\tau) & t > s+\varepsilon \end{cases} \quad (3)$$

Fig. 2 (e) shows schematically the expanded (non-ideal) spike shape.

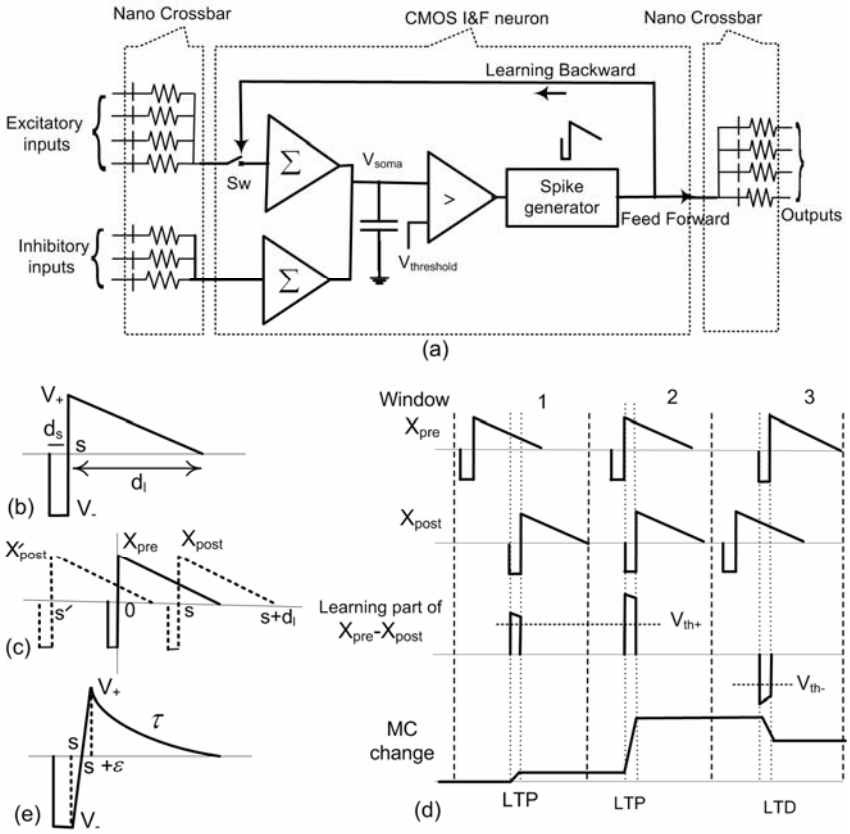

Fig. 2. (a) Neuron structure and basic components (b) Two-part spike that neurons use for learning and processing (c) Pre-and postsynaptic priorities of spikes (d) LTP and LTD learning rates (e) Expanded spike shape.

4 Verifying STDP curves

Using memristive model as (1) and proposed spike shapes, in this section we verify the STDP curves which will result in discussed neural structure. The results of STDP curves are shown in Fig. 3, where the vertical axis shows the average MC change per d_s (the wider the narrow parts, the greater the final LTP and LTD). The spike parameters are scalable and can be adjusted by a control voltage (or current). Memristive parameters, as was mentioned before, depend upon different manufacture conditions. Here, the default spike

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parameters are $V_{\pm} = \pm 0.5\,v$, $\mathrm{d_l} = 10\,\mathrm{ms}$, $\mathrm{d_s} = 0.2\,\mathrm{ms}$ and results are provided for memristives with $V_{th\pm} \approx \pm 0.55\,v$. It is seen that the time length of the learning window is almost equal to $\mathrm{d_l}$ for both LTP and LTD parts.

Fig. 3 (a) shows STDP curves produced by the piecewise linear spike, defined by (2). The results are provided for memristives with three different values of A and B. The resulted STDP curves are superimposed on the conventional 'exp-like' STDP curves, because the $sinh(Bv)$ with $Bv > 1$ is very close to $1/2\ exp(Bv)$.

Fig. 3 (b) shows an example STDP curve produced by the expanded spike, defined by (3), with $\varepsilon = 0.2\,ms$ and $\tau = 4\,ms$. It is seen that in this non-ideal case the resulted curve still has STDP properties and the provided learning window has acceptable duration.

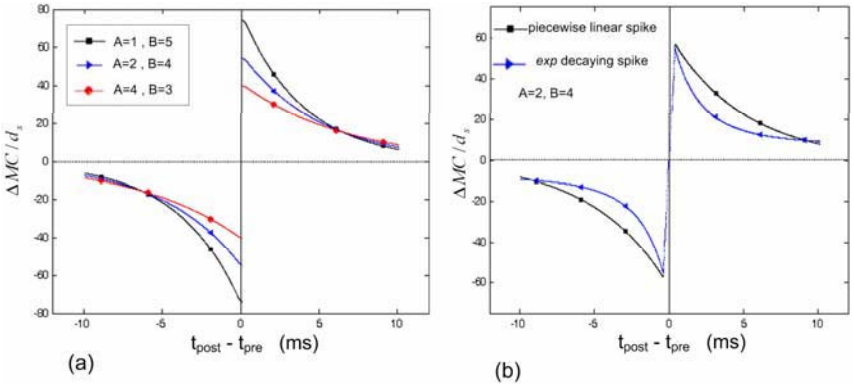

Fig. 3. STDP learning curves (a) using piecewise linear spike and (b) example plot using expanded (non-ideal) spike.

5 Conclusion

Using memristive nanodevice in CMOL architecture and a two-part spike, we have been able to demonstrate STDP learning implementation. From the computational view point, the presented learning method is scalable and reliable. The special shaped spike has a vital role in the proposed learning method, and simulation results show that even non-ideal shapes don't destroy the general trend of STDP curve for LTP and LTD. This would help us to simplify the neuron circuit design.

We suggest the learning method for implementation in crossbar-based CMOS-Nano hardwares, which requires neither significant computational resources nor additional memory to store spike-timing information through time windows.

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